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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/670,036

09/23/2003

Michael D. Flasz

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01/26/2005

WOOD, PHILLIPS, KATZ, CLARK & MORTIMER
500 W. MADISON STREET
SUITE 3800
CHICAGO, IL 60661

EXAMINER

ENGLUND, TERRY LEE

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/670,036	Applicant(s) FLASZA, MICHAEL D.	
	Examiner Terry L Englund	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 September 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character “24” has been used to designate both a wire (e.g. see page 5, line 19) and a housing (e.g. see page 6, line 9). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: Clarification is requested with respect to how control circuit 26 “of any known design” (see page 7, lines 4-6) and control block 38 (see page 7, lines 12-14), can actually perform their function. Using the applicant’s own Fig. 1 as a reference, it is understood that control circuit 26 is coupled between voltage V3 and ground, provides control signal 36, and has some type of connection to primary element 14. However, it is not understood what this control circuit can be, and how control signal 36 and the connection to 14 relate to one another. For example, a simple two resistor voltage divider can provide a control signal from between the two resistors, wherein the connection to 14 could possibly be to either V3, or control signal 36. Control 38 is known to be

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coupled between power supply 22 (at node 16) and ground, with another connection to node 18, and an input receiving control signal 36. It is believed control 38 could be a comparator coupled between 16 and ground for power, receiving the potential at node 18 as a reference signal, and receiving control signal 36 as the variable/comparison signal. However, it is not understood how control 38 actually controls the current through the loop. Does control 38 have an output that controls current source 40, and/or somehow controls the switching within U1 and U2? As presently shown and described, it is understood control 38 is coupled in parallel with respect to power supply 20 and sense resistor R, wherein current source 40, charge pump circuits U1 and U2, and control circuit 26 are also coupled in parallel with 20 and R. Therefore, from the figure, and lack of specific details within the description, it is not understood how loop current I1 would be affected by control 38. Appropriate corrections and/or clarifications required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-20 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. How the loop current is actually controlled is critical or essential to the practice of the invention. Therefore, this current control limitation included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). Although control block 38, shown in Fig. 1, allegedly controls the loop current, the description and the circuit shown in Fig. 1 do not indicate how that is actually performed. As described above with respect to the disclosure and Fig. 1, control 38 does not appear to actually affect the

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loop's current since control 38 is simply shown connected between node 16 and ground, and in parallel with 20/R as well as with 40/U1/U2/26. This type of configuration does not provide sufficient information to how the loop current will be controlled. For example, does control 38 control only current source 40, one or both of the charge pump circuits U1 and U1, or some combination of these elements?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

In so far as being understood, claims 1, 4, 8, 15, 16, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Saito et al. (Saito). Fig. 10 shows a loop powered process instrument comprising control circuit 307 measuring a process variable (e.g. current) and developing control signal 1021 representing the variable; output circuit 1011,1013 is connected to a two-wire loop (e.g. wires 306 and 308) for effectively controlling the loop current (via control of 1018); and power supply circuit 105,1018 is connected to output circuit 1011,1013 and to control circuit 307, wherein 105,1018a receives power from the two-wire process loop and supplies power DCOUTL to control circuit 307. Figs. 11 and 12 each show an example of 1018 having cascaded charge pump circuits between HVIN and DCOUTL. Therefore, claim 1 is anticipated. Since current source 105 effectively connects the cascaded charge pump circuits (within 1018) to output circuit 1011,1013, claim 4 is anticipated. Interpreting Fig. 10 in a

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slightly different manner, current source 105 provides a select current (e.g. the current flowing through 105) to the plurality of cascaded switched capacitor voltage dividers within 1018, thus anticipating claim 8. Fig. 12 shows the capacitor voltage dividers comprising CMOS switched capacitor voltage converters having pump capacitance and output capacitance (e.g. see CPT1 and CPT2), anticipating claim 15. Since 1018 comprises a plurality of cascaded switched capacitor voltage dividers, claims 16 and 18 are anticipated for the same reasons as applied above to corresponding claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2, 5, 9, 12, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (Saito) in view of their respective independent claim 1, 8, or 16. As previously described, Saito shows a loop powered process instrument that reads on the limitations, as far as being understood, recited within the independent claims. However, the reference does not clearly disclose the charge pump circuits/cascaded switched capacitor voltage dividers as divide-by-two circuits, or a regulator diode being connected to the output, as recited within some of the claims. Saito discloses the circuits shown in Figs. 11 and 12 are step-down circuits (e.g. see column 12, lines 21-22 and column 13, lines 27-28), and therefore it is understood they are divide type circuits. It would have been obvious to one of ordinary skill in the art to use divide-by-two type circuits within 1018 if the desired output voltage is required to be HVIN divided by

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a multiple of two. Therefore, claims 2, and 9 are rendered obvious. Also, if several different output voltages are required for various circuitry, each circuit could provide its own corresponding divided voltage. It also would have been obvious to one of ordinary skill in the art to add a regulator diode to output DCOUTL, rendering obvious claims 5, 12, and 20 obvious. The diode would help ensure output DCOUTL is stabilized (or clamped) to minimize adverse affects (e.g. noise) created by the switching operations within 1018.

Claims 3, 7, 10-11, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (Saito) in view of their respective independent claim 1, 8, or 16. As previously described, Saito shows a loop powered process instrument that reads on the limitations recited within the independent claims. However, the reference does not clearly disclose the efficiency of the circuit(s) or dividers. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide circuits or dividers with an efficiency of 90% or 95%, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Also, it is known to one of ordinary skill in the art that switching capacitor circuits can have high efficiency, and what efficiency is required depends on particular applications the circuit will be used in. Therefore, claims 3, 7, 10-11, and 14 are rendered obvious for the above reasons. Claim 17 is rendered obvious for the same efficiency reasoning as described above, along with the same reasoning with respect to the divide-by-two description above (e.g. see the rejections of claims 2, and 9).

No claim is allowable.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least some of the claimed limitations. Tanabe shows a loop instrument in Fig 4a comprising control circuit R11,R12; output circuit 11,10b, and power supply circuit 10 comprising a voltage divider (charge pump or switched capacitor circuit). The control of the switching phases will effectively control the current flowing through the loop. Fig. 2 of Walter shows a loop instrument comprising control circuit 26a,26b; output circuit 45,41,43 for controlling the loop current; and power supply circuit 18 comprising a charge pump or switched capacitor circuit. Although these two references do not show cascaded circuits/dividers, it would have been obvious to one of ordinary skill in the art to use them, depending on what input voltage and output voltage are available or desired. Fig. 1 of Suzuki et al. shows a loop instrument comprising control circuit R1,R2; output circuit 15,13,16; and power supply circuit S1-S4,C1 comprising a charge pump or switched capacitor circuit. The control of the switching phases will effectively control the current flowing through the loop. Suzuki does not show cascaded circuits, but does disclose that a "multiple stage circuit" could be arranged according to the input/output voltages (e.g. see column 4, lines 19-24). Although none of these references was used in any formal rejections described above, each of these references should be carefully reviewed and considered with respect to at least the basic limitations recited.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

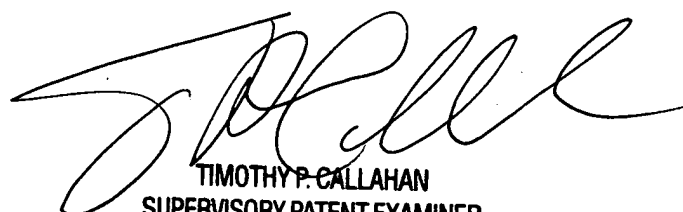
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Terry L. Englund

23 January 2005



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SUPERVISORY PATENT EXAMINER
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